REMARKS

This is intended as a full and complete response to the Office Action dated June 15, 2006, having a shortened statutory period for response set to expire on September 15, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-28 are pending in the application. Claims 1-30 remain pending following entry of this response. Claims 6 and 10 have been amended. New claims 29 and 30 have been added to recite aspects of the invention. Applicants submit that the amendments and new claims do not introduce new matter.

Claim Rejections - 35 USC § 112

Claims 6 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Claim 6 and 10 have been amended to include structural connections, as suggested in the Office Action and, Applicants submit, these claims particularly point out and distinctly claim the subject matter which applicants regard as the invention. Accordingly, Applicants respectfully request withdrawal of this rejection.

Claim Rejections - 35 U.S.C. § 102

Claims 1-5, 7-9 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Koshikawa (US 5428299). Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9

USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case *Koshikawa* does not disclose "each and every element as set forth in the claim." For example, regarding independent claims 1 and 7, *Koshikawa* does not disclose *a test terminal coupled to a test circuit in order to provide an activation signal activating the test circuit to perform a test function and a switching device to selectively couple the test terminal to the internal voltage line during testing of the first circuit.* In fact, *Koshikawa* does not teach any type of test circuit that operates in the claimed manner. In contrast, *Koshikawa* teaches monitoring an external voltage and activating a built-in voltage generator when the external voltage reaches a prescribed range. *See Kosikawa*, Abstract; *See also Kaoshikawa*, Column 4 line 55 – Column 5 Line 24.

The Examiner states that *Koshikawa* discloses, in Figure 5, a first circuit [26 with 22] to be tested, the first circuit comprising an internal voltage line [Vint], a test circuit [23] for testing the first circuit, a test terminal [Pext] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function, and a switching device [24] to selectively couple the test terminal to the internal voltage line during testing of the test circuit [column 8 lines 55-68 and fig. 6].

However, the cited portions are directed at a voltage monitoring circuit for a built-in step-down voltage generator. *Koshikawa* does not disclose testing the built-in step-down voltage generator, nor is the internal reference voltage generator [23] disclosed in *Koshikawa* a test circuit. The Pext terminal in figure 5 is a power supply pin used to connect to an external power voltage Vext in order to power the entire semiconductor chip [column 5 lines 64-68]. The Pext pin is not a test terminal coupled to a test circuit and is not selectively coupled to an internal voltage line during testing of the test circuit as claimed in the current invention. The voltage pre-monitoring circuit [24] has a single input line and a single output line and therefore is not capable of selectively coupling a test terminal to a test circuit, which would require the addition of at least two input or output lines respectively.

Accordingly, Applicants respectfully submit that *Koshikawa* does not teach each and every element as set forth in the claims 1 and 7. Accordingly, Applicants submit claims 1 and 7, as well as their dependents, are allowable and withdrawal of the rejection is respectfully requested.

Claims 1-3 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by *Schnabel* (US 6788087).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case Schnabel does not disclose "each an every element set forth in the claim." For example, regarding claim 1, and the claims that depend therefrom, *Schnabel* does not disclose "a switching device to selectively couple the test terminal to the internal voltage line during testing of the first circuit." The Examiner argues that *Schnabel* discloses a switching device (as a combination of elements 11, 12 and 8) which selectively couples the test terminal (pad 5) to the internal voltage line (voltage line of 2) during testing of the first circuit in Figures 1-2. However, the cited figures and corresponding passages are in fact directed to test terminals (i.e., pads 5) which are constantly connected (i.e., before, during and after testing procedures) via the signal lines 4 to the memory circuit 2. (*See Schnabel* Col. 4, Lines 1-2, 54-55 and Figs. 1 and 2). The elements 11, 12 and 8 of *Schnabel* which the Examiner cites as the "switching device" do not "selectively couple the test terminals to the internal voltage line during testing of the first circuit" as claimed because the test terminals (pads 5) are always connected to the memory circuit 2 regardless of whether the circuit is being tested or being operated in normal operation. There is no suggestion in *Schnabel* that the

address bus lines [7], which are signal lines, can be selectively connected to the internal voltage line of the memory.

Furthermore, *Schnabel* does not disclose any supply level lines related to its disclosed subject matter such as "an internal voltage line" as claimed. The Examiner simply states "voltage line of 2" as "an internal voltage line" as claimed. However, *Schnabel* does not disclose that the memory circuit 2 includes any internal voltage lines (i.e., internal supply level lines) which are connected to the test terminals (pads 5). *Schnabel* clearly states that the "signal lines 4" which are constantly connected to the pads 5, via which to the bus lines 7, are signal level lines (e.g., address lines and data lines) instead of supply level lines. (*Schnabel,* Col. 4, lines 53-58.) Therefore, *Schnabel* does not disclose "a switching device to selectively couple the test terminal to the internal voltage line during testing of the first circuit."

Accordingly, Applicants respectfully submit that the cited sections of *Schnabel* do not teach each and every element as set forth in the claim. Withdrawal of the rejection is respectfully requested.

With respect to claim 23, *Schnabel* does not disclose activating a first switch to couple the test terminal to the internal voltage line after application of the activation signal, whereby the internal voltage line is provided with external power for the testing. As described above, *Schnabel* discloses a constant electrical connection between the pads 5 and the signal lines 4 and no switch is activated to provide this constant connection. Therefore, *Schnabel* does not disclose "activating a first switch to couple the test terminal to the internal voltage line after application of the activation signal, whereby the internal voltage line is provided with external power for the testing."

Accordingly, Applicants respectfully submit that *Schnabel* does not teach each and every element as set forth in the claim. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 7-11, 12, 16-19, 23-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Van Brunt* (US 4357703) in view of *Tada et al.* (US 4801871). Applicants respectfully traverse this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143.

The present rejection fails to establish at least the third criteria, as described below. For example, even if combined as suggested in the Office Action, the references fail to teach selectively coupling a test terminal to an internal voltage line, or a switching device coupled to an output of the test circuit and configured to selectively couple the test terminal to the internal voltage line, as recited in the claims.

The Examiner states that *Van Brunt* discloses a test circuit (elements 40, 20, and 22), a test terminal (elements 21), and a switching device (element 23) coupled to an output of the test circuit and configured to selectively couple (using element 40) the test terminal to the internal voltage line (of item 11) in response to a switching signal from the output. However, the cited portions are in fact directed to a test data input 21 which only acts as a data input to a control shift register 40 (*See* Figure 1) and which is not selectively coupled to an internal voltage line (*e.g.,* of item 11) as asserted by the Examiner. The elements in *Van Brunt* cited by the Examiner are directed to transmission of data signals via signal level lines and inputs (e.g., signal lines 12 and test data pin 21 of *Van Brunt*). Furthermore, *Van Brunt* does not disclose that the "main function circuit 11" includes any internal voltage lines (i.e., internal supply level lines) which are selectively coupled to the test terminal (input 21 of *Van Brunt*).

Accordingly, the cited references do not teach or suggest all the claim limitations as asserted by the Examiner. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Schnabel* as applied to claim 1 above, and further in view of *Horiguchi et al.* (US 5347492). Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Van* and *Tada* as applied to claims 7 and 16 above, and further in view of *Horiguchi et al.* (US 5347492).

Applicants respectfully submit, however, that these claims depend (directly or indirectly) from claims 1, 7 and 16 which Applicants submit are allowable for reasons discussed above. Therefore, these claims are also believed to be allowable, and withdrawal of this rejection is respectfully requested.

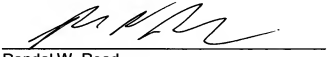
Allowable Subject Matter

Claims 5-6, 14-15, 21-22, 26 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants acknowledge the allowable subject matter and agree these claims are allowable. However, Applicants submit that the base claims from which these claims depend are allowable. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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